Amendments to the claims

The following list of claims replaces all previous versions of claims. Applicants have amended claims, marked as currently amended, without prejudice.

1. (Currently Amended) A method of manufacturing a printed circuit board comprising the steps of:

preparing an insulating substrate having a front surface and a back surface, and a layer of metal foil formed on each of said front surface and said back surface;

selectively forming a plating layer ~~for forming a land~~ on at least one area of at least one of said metal foils, said area covered by said plating layer forming a land;

adjusting a thickness of said plating layer; and

forming areas of said metal foils not covered by said plating layer into lines, said metal foils having at least one area covered by said plating layer.

2. (Original) The manufacturing method according to Claim 1, wherein said adjusting step includes a step of polishing a surface of said plating layer.

3. (Original) The manufacturing method according to Claim 1, further comprising the steps of:

forming a dielectric layer on said insulating substrate, said land and said lines;

forming an opening in said dielectric layer on said land; and

performing plating on said opening.

4. (Original) The manufacturing method according to Claim 2, further comprising the steps of:

forming a dielectric layer on said insulating substrate, said land and said lines;

forming an opening in said dielectric layer on said land; and

performing plating on said opening.

5. (Currently Amended) A method of manufacturing a printed circuit board comprising the steps of:

preparing an insulating substrate having a front surface and a back surface, and a layer of metal foil formed on each of said front surface and said back surface;

forming an opening in at least one of said metal foils and said insulating substrate;

forming a first resist pattern on said metal foil;

forming a plating layer on an inner surface of said opening and the exposed metal foil not covered by said first resist pattern;

adjusting a thickness of said plating layer on said metal foil; and

forming areas of said metal foil not covered by said plating layer into lines, said metal foil having at least one area covered by said plating layer.

6. (Currently Amended) The manufacturing method according to Claim 5, wherein said step of forming said areas of said metal foil into lines comprising the steps of:

removing said first resist pattern;

forming a second resist pattern on said areas of said metal foil ~~and said plating layer~~;

selectively forming an exposed portion of said areas of said metal foil using said second resist pattern;

etching said metal foil at said exposed portion; and

removing said second resist pattern.

7. (Original) The manufacturing method according to Claim 6, further comprising the steps of:

forming a dielectric layer on said insulating substrate and on said plating layer and said lines on said metal foil;

forming an opening in said plating layer; and

performing plating on said opening.

8. (Original) The manufacturing method according to Claim 5, wherein said adjusting step includes a step of polishing a surface of said plating layer.

9. (Original) The manufacturing method according to Claim 6, wherein said adjusting step includes a step of polishing a surface of said plating layer.

10. (Original) The manufacturing method according to Claim 7, wherein said adjusting step includes a step of polishing a surface of said plating layer.

11. (Original) The manufacturing method according to Claim 8, wherein said step of polishing includes polishing using a belt sander or a buff.

12. (Original) The manufacturing method according to Claim 9, wherein said step of polishing includes polishing using a belt sander or a buff.

13. (Original) The manufacturing method according to Claim 10, wherein said step of polishing includes polishing using a belt sander or a buff.

14. (Withdrawn) A printed circuit board comprising:

an insulating substrate having a front surface and a back surface;

a line of metal foil selectively formed on at least one of said front surface and said back surface;

a land selectively formed on at least one of said front surface and said back surface, said land being formed of a stack of said metal foil and a plating layer;

a dielectric layer formed on an exposed portion and said line; and

a via hole formed on said land.